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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/776,981	02/05/2001	Ming-Hau Lee	MORPH1140	2432

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EXAMINER	
CHANG, ERIC	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 05/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/776,981	LEE ET AL.	
	Examiner	Art Unit	
	Eric Chang	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

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DETAILED ACTION

1. Claims 1-15 are pending.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,907,148 to Morton, in view of U.S. Patent 5,892,729 to Holder, Jr.

4. As to claim 1, Morton discloses a method for operating an MxN array of processor cells, comprising: providing a row mask signal configured to enable selected cells in each row of the array [col. 3, lines 20-51]; providing a column mask signal configured to enable selected cells in each column of the array [col. 3, lines 20-51]; to activate the enabled cells in the array based on the row mask signal and column mask signal [col. 3, lines 20-51].

Morton teaches the limitations of the claim, including selecting cells within an array for activation, but does not teach gating the row mask signal and column mask signal with a clock signal of each cell to activate, at the next clock cycle, the enabled cells in the array based on the row mask signal and column mask signal.

Holder teaches that an array of memory cells may be enabled by decoded row-and-column addressing means as is well known in the art [FIGS. 5 & 6, and col. 3, lines 21-25]. Thus, Holder teaches an array of selectively enabled memory cells similar to the array of

selectively activated processor cells of Morton. Holder further teaches gating the address for the cells to be activated with a clock signal for said cell [col. 3, lines 11-29], in order to conserve power [col. 2, lines 5-36].

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ the selective clocking means as taught by Holder. One of ordinary skill in the art would have been motivated to do so that power can be conserved by not clocking elements of a computer array when said elements are not active.

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of selectively enabling a subset of an array of elements within a computer processor. Moreover, the selective clocking means taught by Holder would allow for smaller circuits implementing the teachings of Morton because it allowed for improved heat dissipation [col. 2, lines 28-36].

5. As to claim 2, Morton discloses broadcasting a context instruction to each enabled cell [col. 1, lines 53-58].

6. As to claim 3, Morton discloses executing, during the clock cycle, the context instruction with only the activated cells in the array [col. 1, lines 64-68, and col. 2, lines 1-5].

7. As to claim 4, Morton discloses updating the row mask signal and the column mask signal during each clock cycle [col. 1, lines 64-68, and col. 2, lines 1-5]. Because each

instruction is issued on a new clock cycle [col. 3, lines 39-51], the masking means for selectively activating the enabled cells is likewise updated during each clock cycle.

8. As to claim 5, Morton discloses a method for operating an MxN array of processor cells, wherein each cell is configured to execute a context instruction when active, the method comprising: masking the array to enable a subset of cells of the array [col. 3, lines 20-51]; and activating each enabled cell to execute the context instruction [col. 3, lines 39-51]. Holder teaches disabling unselected cells in the array, such that each disabled cell does not consume power [col. 2, lines 5-36].

9. As to claim 6, Morton discloses an MxN array of processor cells, comprising: a row mask register configured to provide a row mask signal for enabling selected cells in each row of the array [col. 3, lines 20-51]; and a column mask register configured to provide a column mask signal for enabling selected cells in each column of the array [col. 3, lines 20-51. Holder teaches a clock circuit, connected to supply each cell with a clock signal, each clock signal being gated with an enable signal to activate the enabled cells upon a new clock cycle [col. 3, lines 11-29 and 45-55].

10. As to claims 7-8, Morton discloses the row and column mask registers are M-bit and N-bit registers [col. 1, lines 49-52, and col. 3, lines 31-36], wherein the masks correspond to the rows and columns in the processor [col. 3, lines 39-51]. It would further be obvious to one of

ordinary skill in the art that the mask signals from such registers would have M-bit and N-bit width, substantially as claimed.

11. As to claim 9, Morton discloses a mask generator for generating the signal to the row and column mask registers [FIG. 1, element 15, and col. 3, lines 20-31].

12. As to claim 10, Morton discloses a context instruction generator for generating and supplying a context instruction to each enabled cell for execution when the cell is activated [col. 1, lines 53-58].

13. As to claim 11, Morton discloses an MxN array of processor cells, comprising: a mask circuit for generating a mask signal for masking a portion of the cells in the array [col. 3, lines 20-51]. Holder teaches a clock for providing a clock signal, the clock signal being gated with the mask signal to activate the masked cells upon a new clock cycle [col. 3, lines 11-29 and 45-55].

14. As to claim 12, Morton discloses a row and column mask register connected to a row and column of cells, respectively [FIG. 1, and col. 3, lines 20-51].

15. As to claim 13, Morton discloses the row and column mask registers are M-bit and N-bit registers [col. 1, lines 49-52, and col. 3, lines 31-36], wherein the masks correspond to the rows and columns in the processor [col. 3, lines 39-51]. It would further be obvious to one of ordinary

skill in the art that the mask signals from such registers would have M-bit and N-bit width, substantially as claimed.

16. As to claim 14, Morton discloses the row and column signals are gated together at an input to each cell [col. 3, lines 39-51]. Morton teaches that the cells at the intersection of the row and column signals are enabled and disabled according to said signals.

17. As to claim 15, Morton discloses the mask signal is configured to enable the masked cells [col. 3, lines 39-51].

Response to Arguments

18. Applicant's arguments with respect to claims 1-15 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Chang whose telephone number is (571) 272-3671. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

April 29, 2005
ec

LYNNE H. BROWNE
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